PVI Systems Chameleon for PXI Above 2MHz Acquisition

Overview

Chameleon PXI version 1.8.3 has been modified to enable high speed data acquisition above 2M/samples per second. Certain features and functions of Chameleon had to be modified to enable this much higher speed than normal and they are listed in this document as well as the NI hardware used in making these changes.

Hardware Setup

The hardware used to develop and test the high speed acquisition is as follows:

Function	Model	Description
PXI Chassis	NI PXIe-1082	8 slot PXIe Chassis 4GB bandwidth
PXI Computer	NI PXIe-8133	Intel i7 PXI Computer, 8GB Ram, 500GB SSD
Data Acq Card (Qty 2)	NI PXIe-4481	6 channel 24bit Analog Input Module – Max Speed 20MS/s
Timing Card	NI PXIe-6674T	PXIe Synchronization Module used to generate a high speed stable clock and to capture the digital trigger input for the Digital PreTrigger mode in the Chameleon Software
Signal Generator	Mercer 9805	Used to generate a common sine wave input to the 2 NI PXIe-4481 modules

Software Modifications to Support High Speed (>2MHz)

Chameleon has the ability to display and monitor for alarms which has been disabled for speeds greater than 2MHz. This was done to handle the increased load on the software at these higher sample rates.

It is recommended that customers setup two (2) Chameleon configurations in order to capture data above 2MHz.

1. A configuration with all the desired channels with a sampling rate of approximately 1MHz so that the signal connections may be tested and viewed using chameleons display and monitoring functions. The acquisition mode could be set to free running as opposed to triggered which would be used for the higher sample rates
2. A configuration with all the desired channels with the desired sampling rate above 2MHz. This would use the acquisition mode of either Digital Triggering or Digital Pre-Triggering.

Tested Acquisition Speeds Greater than 2MHz

Chameleon PXI was tested at the following configurations:

Number of Channels	Sample Rate	Pre-Trigger Buffer	Post Trigger Buffer
12	2 MHz	0.2 Seconds	10 Seconds
12	3.33 MHz	0.2 Seconds	10 Seconds
12	4 MHz	0.2 Seconds	10 Seconds
12	5 MHz	0.2 Seconds	10 Seconds
12	6.66 MHz	0.2 Seconds	10 Seconds
12	10 MHz	0.2 Seconds	10 Seconds

It should possible to acquire more channels at speeds less than 10MHz since the load is less on the system but the exact amount of channels is not clear since we did not have the capacity to test beyond 12 channels.

The number of channels could also be increased by using a faster computer with more ram.

It was assumed that the event being captured we of a short duration, <10seconds, and that a digital trigger was being used to indicate the start of the event.

Revision History

Revision	Date	Author	Comment
1.0	23 January 2023	William Schramm-PVI	Initial Release